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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,924	05/30/2001	Nobuaki Hashimoto	109681	6373

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER
TRAN, TAN N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/856,924	Applicant(s) HASHIMOTO ET AL.	
	Examiner TAN N TRAN	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 02/06/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-9 and 13-15* is/are allowed.

6)☒ Claim(s) *1-6,10-12 and 16-19* 33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6,10-12,16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuka (US 5,949,142) in view of Grupen-Shemansky et al. (6,022,761).

With regard to claim 1, Otsuka. discloses a substrate 4 including a plurality of holes and a surface over which an interconnecting pattern 4b is formed, part of the interconnecting pattern 4b being superposed over the holes; a semiconductor chip 2 disposed over another surface of the substrate 4 and including a plurality of electrodes to be positioned over the holes; and conductive posts (4a,4c) comprise interlevel conductive bump provided on the electrode 2a within the holes to be electrically connect to the interconnecting pattern 4b. (Note lines 67, column 4 and lines 1-5, column 5, figs 1, 3 of Otsuka)

Otsuka does not disclose conductive posts provided contiguously on the electrodes.

However, Grupen-Shemansky et al. discloses the conductive bumps (13,21) provided contiguously and directly contact to the electrode 27. (Note fig. 4 of Grupen-Shemansky et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Otsuka's device having the conductive bumps provided contiguously and directly contact to the

electrode such as taught by Grupen-Shemansky et al. in order to minimize the overall thickness of the finished substrate module.

With regard to claim 2, Otsuka discloses a resin 6 is provided between the substrate 4 and the semiconductor chip 2. (Note figs 1, 3 of Otsuka).

With regard to claim 3, Otsuka discloses the resin is an anisotropic conductive material 6 containing conductive particles 6a. (Note lines 13-17, column 4, figs 1, 3 of Otsuka).

With regard to claim 4, Otsuka. discloses the part of the interconnecting 4b closes the holes. (Note figs 1, 3 of Otsuka).

With regard to claim 5, Otsuka discloses the interconnecting pattern 4b includes a plurality of interconnecting lines; and wherein two or more interconnecting lines extend over each of the holes.

With regard to claim 6, Otsuka and Grupen-Shemansky et al. disclose all claimed invention as in claim 1, except the other surface of the substrate 4 is roughed. However, it would have been obvious to one of ordinary skill in the art to form Otsuka's case having surface of the substrate 4 is roughed because such element 4 is conventional in the art in order to make the resin 6 is more stable.

With regard to claim 10, Otsuka discloses the conductive post (4a, 4c) are a plurality of layered bumps. (Note figs 1, 3 of Otsuka).

With regard to claim 11, Otsuka discloses the bumps (4a, 4c) include first bumps 4a formed on the electrodes and second bumps 4c formed on the first bumps 4a. (Note figs 1, 3 of Otsuka).

With regard to claim 12, Otsuka and Grupen-Shemansky et al. disclose all claimed invention as in claims 1 and 10, except at least the first bumps are ball bumps. However, it would have been obvious to one of ordinary skill in the art to form Otsuka and Grupen-Shemansky et al.'s case having at least the first bumps are ball bumps in order to form the conductive particles in a thermosetting resin for electrically connecting to the semiconductor chip via an insulating layer more easy.

With regard to claim 16, Otsuka and Grupen-Shemansky et al disclose all claimed invention as in claims 1 and 11, except the first bumps and the second bumps are formed of the same material. However, it would have been obvious to one of ordinary skill in the art to form Otsuka and Grupen-Shemansky et al's case having the first bumps and the second bumps are formed of the same material in order to simplify the processing steps.

With regard to claim 17, Otsuka discloses the semiconductor chip is mounted face-down to the substrate. (Note figs 1, 3 of Otsuka).

With regard to claims 18 and 19, Otsuka and Grupen-Shemansky et al disclose all claimed invention as in claim 1, except a circuit board and electronic instrument provided with the semiconductor device. However, it would have been obvious to one of ordinary skill in the art to form Otsuka and Grupen-Shemansky et al's case on a circuit board or an electronic instrument provided with the semiconductor device because such structure is conventional in the art for forming the semiconductor integrated circuit package.

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuka (US 5,949,142) in view of Grupen-Shemansky et al. (6,022,761) and further in view of Kim et al. (2002/0003308).

Otsuka and Grupen-Shemansky et al do not disclose there is a space between each of the conductive posts and an inner surface of each of the holes.

However, Kim et al. discloses there is a space between a conductive post 33 and an inner surface of each of the holes 22. (Note fig. 9 of Kim et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Otsuka and Grupen-Shemansky et al's device having there is a space between each of the conductive posts and an inner surface of each of the holes such as taught by Kim et al in order to reduce warpage of the package.

Allowable Subject Matter

2. Claims 7-9, 13-15 are allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as a recognition hole is formed in the substrate at position differing from the holes; and wherein a recognition pattern is formed over the recognition hole on the side of a surface of the substrate including the interconnecting pattern in claim 7, and the second bumps are formed of a metal which has a melting point lower than the melting point of the first bumps in claim 13.

Response to Arguments

3. Applicant's arguments filed 02/06/03 have been fully considered but they are not persuasive.

It is argued, at pages 2,3 of the remarks, that "Otsuka fails to teach or suggest a semiconductor device including "conductive posts provided contiguously on the electrode and within the holes to be electrically connected to the interconnecting pattern" and "Otsuka fail to teach or suggest that the conductive posts (4a,4c) are provided contiguously on, or touching, the electrode 2a and within the holes to be electrically connected to an interconnecting pattern". However, lines 67, column 4, lines 1-5, column 5, and figs 1, 3 of Otsuka do show at least conductive posts (4a,4c) provided on the electrodes 2a and within the holes to be electrically connected to the interconnecting pattern 4b; and fig. 4 of Grupen-Shemansky et al. does show the conductive bumps (13,21) provided contiguously and directly contact to the electrode 27. Therefore, it would have been obvious to one of ordinary skill in the art to form the Otsuka's device having the conductive bumps provided contiguously and directly contact to the electrode such as taught by Grupen-Shemansky et al. in order to minimize the overall thickness of the finished substrate module. Thus, Applicant's claim 1 does not distinguish over Otsuka and Grupen-Shemansky et al. references.

It is argued, at page 3 of the remarks, that "Kim fails to cure the deficiencies of Otsuka discussed above with respect to independent claim 1". However, In response to applicant's

arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

Mar 2003

Minh Loan Tran
Primary Examiner